REMARKS

Present Status of the Application

The office action rejected claims 1, 3, 7-9, and 11-13 under 35 U.S.C. 103(a) as being unpatentable over Kawauchi (US 5,619,653) in view of Giroir et al (US 4,980,852, hereinafter "Giroir") Nanba (US 4,665,484) and Fujimoto (US 5,418,913).

The office action rejected claims 2 and 10 under 35 U.S.C. 103(a) as being unpatentable over Kawauchi, in view of Giroir, Nanba and Fujimoto, and further in view of Fried et al (US 5,142,676).

The office action rejected claims 4-6 under 35 U.S.C. 103(a) as being unpatentable over Kawauchi (US 5,619,653), in view of Giroir, Nanba and Fujimoto, and further in view of Balmer et al (US 5,742,599).

The Office Action dated June 09, 2009 has been received and its contents are carefully considered.

In response to the aforesaid rejection, Applicants have amended claims 1, 2, 9 and 10 and added the new claims 21-25 to describe the claimed invention more explicitly. The feature "*the distribution complete flag set by the write control unit and the write complete flag of the target message row are both cleared by the read control unit*" and "*the distribution complete flag has not been cleared by the write control unit before being cleared by the read control unit*" are added into independent claims 1 and 9. Such added features are inherently taught in the specification and the drawings of the present application, especially in paragraphs [0018] and [0019] which teach that

"*the distribution complete flag is used to prevent any previous message that has not been processed yet from being overlapped*" and that "*the distribution complete flag and the write complete flag of the message row 130 are both cleared after the destination controller 120 completes reading the message*". Claims 21 and 23 are added according to the paragraph [0018] of the present application, the claims 22 and 24 are added according to the paragraph [0017] of the present application, and claim 25 is added according to the paragraph [0021] of the present application. No new matter is introduced.

After entry of said amendments, it is respectfully submitted that the pending claims 1-13 and 21-25 are patentably distinguishable over the cited references for at least the following reasons.

Response to Claim Rejections Under 35 U.S.C. 103(a)

As acknowledged by Examiner's Action, the Kawauchi/Giroir system fails to teach the use of a distribution complete flag which is cleared by the read control unit once the destination controller completes reading the message of the target message row, as recited by claims 1 and 9. To overcome this admitted deficiency of the combined system of Kawauchi and Giroir, the Action relies on the teachings of Nanba. However, Applicants believe that there is no suggestion or motivation to make the proposed modification **because the proposed modification would render Nanba unsatisfactory for its intended purpose**. Please refer to MPEP § 2143.01, subsection V, which recites "If proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the

proposed modification". *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984).

As recited in the amended claims 1 and 9 of the present application, the distribution complete flag ***set by the write control unit*** is cleared ***by the read control unit***, and the distribution complete flag has not been cleared by the write control unit before being cleared by the read control unit. Referring to FIG. 1 of the present application, a distribution complete flag (C0-C3) of a target message row (130) is set ***by the write control unit 165*** when the source controller (110) reads an address of the target message row (130), and the distribution complete flag (C0-C3) of the target message row (130) is cleared ***by the read control unit 195*** once the destination controller (120) completes reading the message of the target message row (130). The distribution complete flag (C0-C3) has not been cleared by the write control unit (165) before being cleared by the read control unit (195) so as *to prevent any previous message that has not been processed yet from being overlapped*. In addition, as shown in FIG. 1 of the present application, the plurality of message rows 130 are coupled between the write control unit 165 and the read control unit 195. Therefore, the distribution complete flag (C0-C3) is cleared by the read control unit 195, which is different from the write control unit 165.

However, Nanba teaches that the lock flag/bit, i.e. the first bit of the GATE, **is set and cleared by the same processor** before the shared resource is released. Firstly, according to the specification of Nanba, the first bit of the GATE is used to indicate whether the shared resource is in a locked status or in an unlocked status. The first bit of the GATE is set to "1" if the shared resource is locked, and the first bit of the GATE is set to "0" if the shared resource is unlocked. Secondly, Nanba teaches that "*At step 68, the processor P0 applies the address signal indicative of*

the GATE address via the address bus AB, while applying the data having all bits "1"s to the entire GATE ..... The reason that the all logic "1"s are stored in the entire GATE at step 68, is ***to prevent the other processors from accessing the shared resource which the processor P0 intends to use***" (see col. 4, line 63 to col. 5, line 7) and that "*a program executed on the processor P0 intends to use a shared resource and hence is going to lock same* ***for the exclusive use thereof***" (see col. 4, lines 41-43). Referring to FIG. 2 of Nanba, when the processor P0 uses a shared resource in the main memory 40, the processor P0 sets all bits of the GATE of the shared resource to "1" so as to prevent the other processors P1 and P2 from using the shared resource. Since the other processors P1 and P2 cannot use the shared resource, which is locked by the processor P0, the first bit of the GATE of the shared resource would not be cleared by the other processors P1 and P2. In other words, if Nanba allows the first bit of the GATE being set to "0", i.e. cleared, by the other processor P1 or P2, the shared resource locked by the processor P0 would be released by the other processor P1 or P2 even if the processor P0 still uses the shared resource. In such case, the processor P0 would fail to lock the shared resource ***for exclusive use thereof***, and the program executed on the processor P0 may operate erroneously due to misplacement or overlap of the shared resource.

For at least the foregoing reasons, the first bit of the GATE of Nanba must be set and cleared by the same processor when the shared resource is used exclusively. Otherwise, Nanba will fail to lock the shared resource to prevent other processor from using the shared resource. Therefore, Applicants believe that the teachings of the references are not sufficient to render the claims 1 and 9 obvious **since the proposed modification would render Nanba unsatisfactory for its intended purpose** (i.e. exclusive use of resource).

It is respectfully submitted that independent claims 1 and 9 and their dependent claims of the present application are patented over the cited references. Reconsideration and allowance of the application and presently pending claims 1-13 and 21-25 are respectfully requested.

CONCLUSION

For at least the foregoing reasons, it is believed that all the pending claims 1-13 and 21-25 of the present application patently define over the prior art and are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

Respectfully submitted,
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